Amendments to the Claims

1. (currently amended) A method of forming a semiconductor device, the method comprising the steps of:

forming a charge-trapping dielectric layer over a substrate, the charge-trapping dielectric layer including a tunnelling layer, a charge-trapping layer, and an insulating layer, wherein the tunnelling layer is disposed over the substrate, the charge-trapping layer is disposed over the tunnelling layer and the insulating layer is disposed over the charge-trapping layer;

forming a mask layer over the dielectric layer;

forming a photosensitive layer over the mask layer;

using the photosensitive layer to patterning only the mask layer to form a mask including a mask line and space pattern, the mask line and space pattern including at least one mask space; and

forming a conductive layer over the patterned mask layer and filling in the at least one mask space, the conductive layer including a width dimension about equal to the width dimension of the least one mask space;; and

planarizing the conductive layer down to horizontal surfaces of the mask, and

wherein the substrate comprises

a germanium-on-insulator (GOI) structure including:

a semiconductor substrate;

an insulating layer disposed over the semiconductor substrate; and

a semiconductive layer comprising germanium (Ge) disposed over the insulating layer.

2. (original) The method according to claim 1, further comprising the steps of:

removing the mask to expose sidewalls of the conductive layer, wherein the sidewalls include relatively smooth surfaces.

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3. (original) The method according to claim 1, wherein the mask layer comprises at least one of photoresist; silicon oxide (Si_xO_y), silicon-dioxide (SiO_2), aluminum oxide (Al_2O_3), hafnium oxide (HfO), zirconium oxide (ZrO), titanium oxide (TiO), yttrium oxide (YO), lanthanum oxide (La_2O_3), cerium oxide (CeO_2), bismuth silicon oxide ($Bi_4Si_2O_{12}$), tantalum oxide (Ta_2O_5), tungsten oxide (WO_3), $LaAlO_3$, BST ($Ba_{1-x}Sr_xTiO_3$), $PbTiO_3$, $BaTiO_3$, $SiTiO_3$, $PbZrO_3$, PST ($PbSc_xTa_{1-x}O_3$), PZN ($PbZn_xNb_{1-x}O_3$), PZT ($PbZr_xTi_{1-x}O_3$), PMN ($PbMg_xNb_{1-x}O_3$), binary and tertiary metal oxides, other metal oxides; silicon nitride (Si_xN_y), silicon oxynitride (SiO_xN_y), other nitrides; zirconium silicate, hafnium silicate, other silicates; ferro electric material; the aforementioned materials implanted with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in porous, amorphous, single crystal, polycrystalline, or nanocrystalline form; and mixtures thereof.

4. (original) The method according to claim 1, further comprising the step of:

forming and patterning an anti-reflective coating (ARC) over the mask layer.

5. (original) The method according to claim 4, wherein the mask comprises the patterned ARC and the patterned mask layer.

6-9. (cancelled)

10. (previously presented) The method according to claim 1, wherein the germanium (Ge) comprises crystalline germanium.

11. (cancelled)

12. (cancelled)

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13. (original) The method according to claim 1, wherein the dielectric layer comprises at least one of silicon oxide (Si_xO_y), silicon-dioxide (SiO_2), aluminum oxide (Al_2O_3), hafnium oxide (HfO), zirconium oxide (ZrO), titanium oxide (TiO), yttrium oxide (YO), lanthanum oxide (La_2O_3), cerium oxide (CeO_2), bismuth silicon oxide ($Bi_4Si_2O_{12}$), tantalum oxide (Ta_2O_5), tungsten oxide (WO_3), $LaAlO_3$, BST ($Ba_{1-x}Sr_xTiO_3$), $PbTiO_3$, $BaTiO_3$, $SiTiO_3$, $PbZrO_3$, PST ($PbSc_xTa_{1-x}O_3$), PZN ($PbZn_xNb_{1-x}O_3$), PZT ($PbZr_xTi_{1-x}O_3$), PMN ($PbMg_xNb_{1-x}O_3$), binary and tertiary metal oxides, other metal oxides; silicon nitride (Si_xN_y), silicon oxynitride (SiO_xN_y), other nitrides; zirconium silicate, hafnium silicate, other silicates; ferro electric material; the aforementioned materials implanted with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in porous, amorphous, single crystal, polycrystalline, or nanocrystalline form; and mixtures thereof.

14. (original) The method according to claim 1, wherein the mask defines a pitch of the mask line and space pattern.

15. (original) The method according to claim 2, wherein the step of forming the conductive layer comprises the steps of:

forming a conformal layer of a conductive material over the mask and exposed surface of the dielectric layer; and

anisotropically etching to remove a portion of the conductive material from horizontal surfaces of the mask.

16. (currently amended) A method of forming a semiconductor device, the method comprising the steps of:

forming a charge-trapping dielectric layer over a substrate, the charge-trapping dielectric layer including a tunnelling layer, a charge-trapping layer, and an insulating layer, wherein the tunnelling layer is disposed over the substrate, the charge-trapping layer is disposed over the tunnelling layer and the insulating layer is disposed over the charge-trapping layer;

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forming a mask over ~~a substrate~~ the charge-trapping dielectric layer to include a line and space pattern, the line and space pattern having at least one space including a width dimension; and

forming a conductive layer over the mask layer and filling ~~in~~ the at least one space of the mask, the conductive layer ~~includes~~ including a width dimension about equal to the width dimension of the at least one space of the mask; and

planarizing the conductive layer down to horizontal surfaces of the mask;

~~wherein the substrate comprises~~

~~a germanium-on-insulator (GOI) structure including:~~

~~a semiconductor substrate;~~

~~an insulating layer disposed over the semiconductor substrate; and~~

~~a semiconductive layer comprising germanium (Ge) disposed over the insulating layer~~.

17. (cancelled)

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